WHAT IS CLAIMED IS:

1. A circuit for reducing leakage current in a processor of an electronic apparatus, the processor having a joint test action group (JTAG) test terminal, the circuit comprising:

an initialization test pin included in the JTAG test terminal;

a reset pin of the processor; and

a semiconductor device connected between the initialization test pin and the reset pin, wherein

the initialization test pin, the reset pin, and the semiconductor device are arranged to enable forward current to flow from the initialization test pin to the reset pin through the semiconductor device.

2. The circuit as claimed in claim 1, wherein a diode is connected between the initialization test pin and the reset pin, so that forward bias is applied from the initialization test pin to the reset pin, thereby enabling current to flow through the diode from the initialization test pin to the reset pin.

3. The circuit as claimed in claim 1, wherein a transistor is connected and disposed between the initialization test pin and the reset pin of the processor, so that forward bias is applied from the initialization test pin to the reset pin, thereby enabling current to flow through the transistor from the initialization test pin to the reset pin.

4. The circuit as claimed in claim 3, wherein the transistor is a NPN transistor, a collector terminal of the transistor is connected to the initialization test pin, and an emitter terminal of the transistor is connected to the reset pin.

5. The circuit as claimed in claim 3, wherein the transistor is a PNP transistor, an emitter terminal of the transistor is connected to the initialization test pin, and a collector terminal of the transistor is connected to the reset pin.

6. The circuit as claimed in claim 3, wherein a control signal, which controls current flowing from the initialization test pin to the reset pin, is input to a base terminal of the transistor.

7. The circuit as claimed in claim 1, wherein a Metal-Oxide Semiconductor Field Effect Transistor (MOSFET) is connected and disposed between the initialization test pin and the reset pin of the processor, so that forward bias is applied from the initialization test pin to the reset pin, thereby enabling current to flow through the MOSFET from the initialization test pin to the reset pin.

8. The circuit as claimed in claim 7, wherein the MOSFET is an N channel MOSFET, a drain terminal of the MOSFET is connected to the initialization test pin, and a source terminal of the MOSFET is connected to the reset pin.

9. The circuit as claimed in claim 7, wherein the MOSFET is an P channel MOSFET, a drain terminal of the MOSFET is connected to the initialization test pin, and a source terminal of the MOSFET is connected to the reset pin.

10. The circuit as claimed in claim 7, wherein a control signal, which controls voltage applied from the initialization test pin to the reset pin, is input to a base terminal of the MOSFET.

11. The circuit as claimed in claim 1, wherein the processor having the JTAG test terminal is a modem chip contained in a mobile communication terminal.

12. The circuit as claimed in claim 1, wherein the semiconductor device connected between the initialization test pin and the reset pin of the processor is constructed in the processor chip.